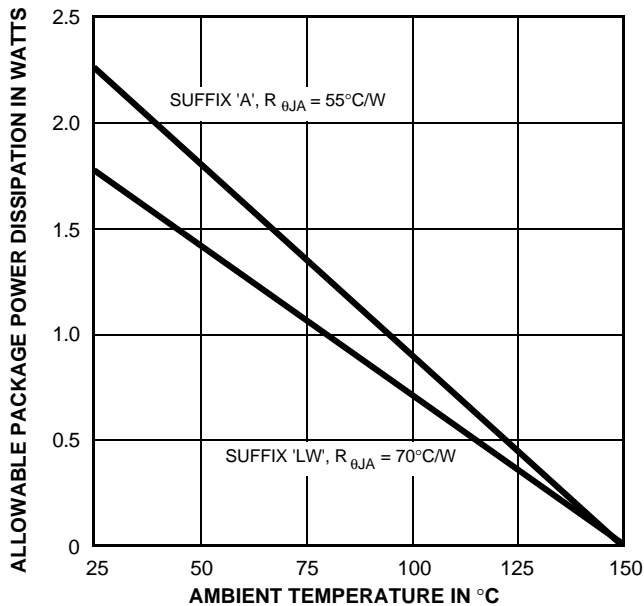


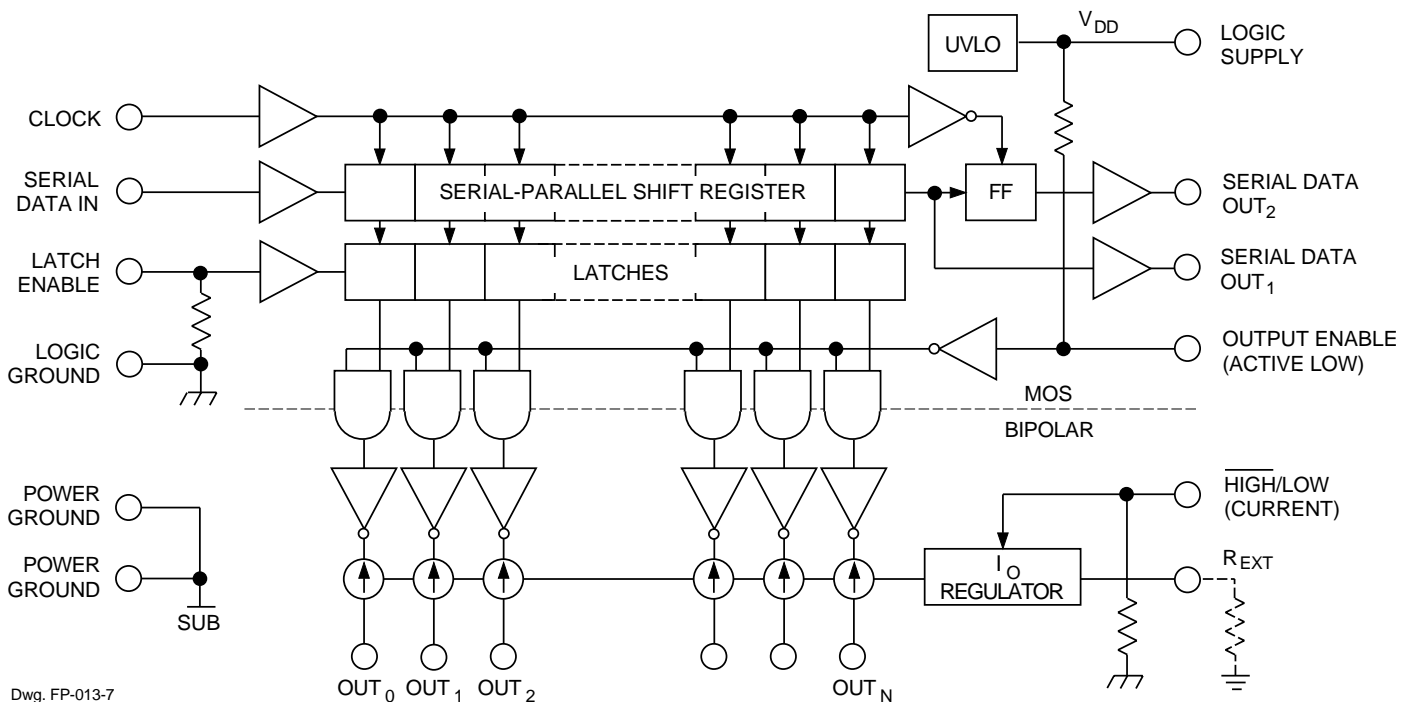
6277

8-BIT SERIAL-INPUT, CONSTANT-CURRENT LATCHED LED DRIVER



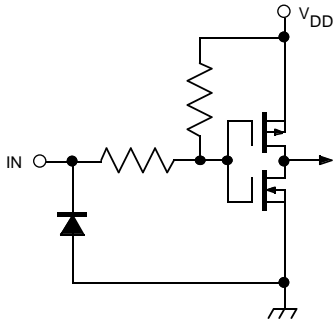
Dwg. GP-018-1

FUNCTIONAL BLOCK DIAGRAM



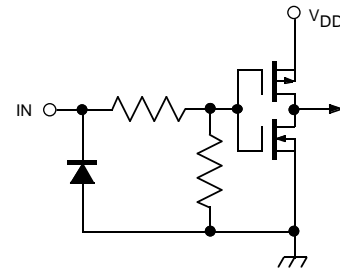
Dwg. FP-013-7

6277 8-BIT SERIAL-INPUT, CONSTANT-CURRENT LATCHED LED DRIVER



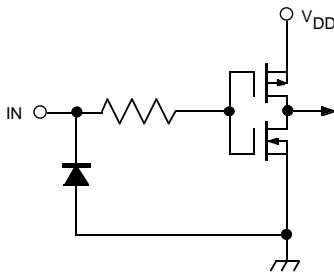
Dwg. EP-010-11

OUTPUT ENABLE (active low)



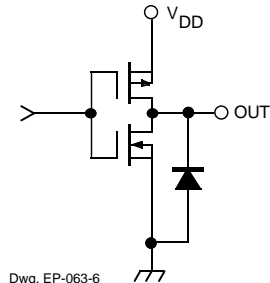
Dwg. EP-010-12

LATCH ENABLE and HIGH/LOW



Dwg. EP-010-13

CLOCK and SERIAL DATA IN



Dwg. EP-063-6

SERIAL DATA OUT

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents					Serial Data Output	Latch Enable Input	Latch Contents					Output Enable Input	Output Contents						
		I_1	I_2	I_3	...	I_{N-1}			I_N	l_1	l_2	l_3	...		l_{N-1}	l_N	o_1	o_2	o_3	...	o_{N-1}
H		H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}													
L		L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}													
X		R_1	R_2	R_3	...	R_{N-1}	R_N	R_N													
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N						
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L					
										X	X	X	...	X	X	H	H	H	...	H	H

L = Low Logic (Voltage) Level H = High Logic (Voltage) Level X = Irrelevant P = Present State R = Previous State

6277

8-BIT SERIAL-INPUT, CONSTANT-CURRENT LATCHED LED DRIVER

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{H/L} = V_{DD} = 5\text{ V}$ (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Unit
Supply Voltage Range	V_{DD}	Operating	4.5	5.0	5.5	V
Under-Voltage Lockout	$V_{DD(UV)}$	$V_{DD} = 0$ to 5 V	3.4	–	4.0	V
Output Current (any single output)	I_O	$V_{CE} = 1.0\text{ V}$, $R_{EXT} = 160\ \Omega$	100	120	140	mA
		$V_{CE} = 0.4\text{ V}$, $R_{EXT} = 470\ \Omega$	34	42	48	mA
Output Current Matching (difference between any two outputs at same V_{CE})	ΔI_O	$0.4\text{ V} \leq V_{CE(A)} = V_{CE(B)} \leq 1.0\text{ V}$: $R_{EXT} = 160\ \Omega$	–	± 1.5	± 6.0	%
		$R_{EXT} = 470\ \Omega$	–	± 1.5	± 6.0	%
Output Leakage Current	I_{CEX}	$V_{OH} = 20\text{ V}$	–	1.0	5.0	μA
Logic Input Voltage	V_{IH}		$0.7V_{DD}$	–	–	V
	V_{IL}		–	–	$0.3V_{DD}$	V
SERIAL DATA OUT Voltage (SDO_1 & SDO_2)	V_{OL}	$I_{OL} = 1.0\text{ mA}$	–	–	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{ mA}$	4.6	–	–	V
Input Resistance	R_I	ENABLE input, pull up	150	300	600	$\text{k}\Omega$
		LATCH & $\overline{\text{HIGH/LOW}}$ inputs, pull down	100	270	400	$\text{k}\Omega$
Supply Current	$I_{DD(OFF)}$	$R_{EXT} = \text{open}$, $V_{OE} = 5\text{ V}$	–	0.8	1.6	mA
		$R_{EXT} = 470\ \Omega$, $V_{OE} = 5\text{ V}$	3.5	6.5	9.5	mA
		$R_{EXT} = 160\ \Omega$, $V_{OE} = 5\text{ V}$	14	17	22	mA
	$I_{DD(ON)}$	$R_{EXT} = 470\ \Omega$, $V_{OE} = 0\text{ V}$	5.0	10	15	mA
		$R_{EXT} = 160\ \Omega$, $V_{OE} = 0\text{ V}$	20	27	40	mA

Typical Data is at $V_{DD} = 5\text{ V}$ and is for design information only.

6277
8-BIT SERIAL-INPUT,
CONSTANT-CURRENT
LATCHED LED DRIVER

SWITCHING CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IH} = 5\text{ V}$, $V_{CE} = 0.4\text{ V}$, $V_{IL} = 0\text{ V}$, $R_{EXT} = 470\ \Omega$, $I_O = 40\text{ mA}$, $V_L = 3\text{ V}$, $R_L = 65\ \Omega$, $C_L = 10.5\text{ pF}$.

Characteristic	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Propagation Delay Time	t_{pHL}	CLOCK-OUT _n	–	350	1000	ns
		LATCH-OUT _n	–	350	1000	ns
		ENABLE-OUT _n	–	350	1000	ns
		CLOCK-SERIAL DATA OUT ₁	–	40	–	ns
Propagation Delay Time	t_{pLH}	CLOCK-OUT _n	–	300	1000	ns
		LATCH-OUT _n	–	400	1000	ns
		ENABLE-OUT _n	–	380	1000	ns
		CLOCK-SERIAL DATA OUT ₂	–	40	–	ns
Output Fall Time	t_f	90% to 10% voltage	150	250	1000	ns
Output Rise Time	t_r	10% to 90% voltage	150	250	600	ns

RECOMMENDED OPERATING CONDITIONS

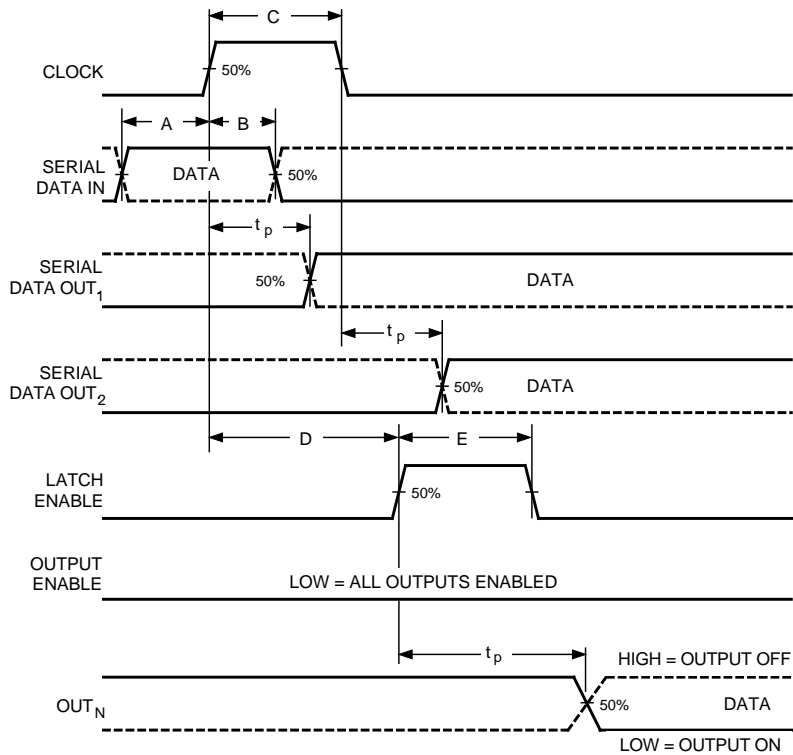
Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Output Voltage	V_O		–	1.0	4.0	V
Output Current	I_O	Continuous, any one output	–	–	150	mA
	I_{OH}	SERIAL DATA OUT	–	–	-1.0	mA
	I_{OL}	SERIAL DATA OUT	–	–	1.0	mA
Logic Input Voltage	V_{IH}		$0.7V_{DD}$	–	–	V
	V_{IL}		–	–	$0.3V_{DD}$	V
Clock Frequency	f_{CK}	Cascade operation	–	–	10	MHz

6277

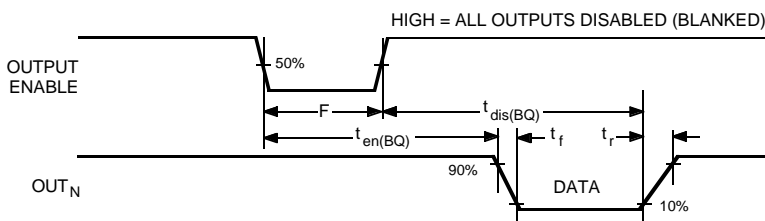
8-BIT SERIAL-INPUT, CONSTANT-CURRENT LATCHED LED DRIVER

TIMING REQUIREMENTS and SPECIFICATIONS

(Logic Levels are V_{DD} and Ground)



Dwg. WP-029-3



Dwg. WP-030-1

- A. Data Active Time Before Clock Pulse**
(Data Set-Up Time), $t_{su(D)}$ **60 ns**
 - B. Data Active Time After Clock Pulse**
(Data Hold Time), $t_{h(D)}$ **20 ns**
 - C. Clock Pulse Width, $t_{w(CK)}$ **50 ns****
 - D. Time Between Clock Activation**
and Latch Enable, $t_{su(L)}$ **100 ns**
 - E. Latch Enable Pulse Width, $t_{w(L)}$ **100 ns****
 - F. Output Enable Pulse Width, $t_{w(OE)}$ **4.5 μ s****
- NOTE – Timing is representative of a 10 MHz clock.
Significantly higher speeds are attainable.
- Max. Clock Transition Time, t_r or t_f **10 μ s**

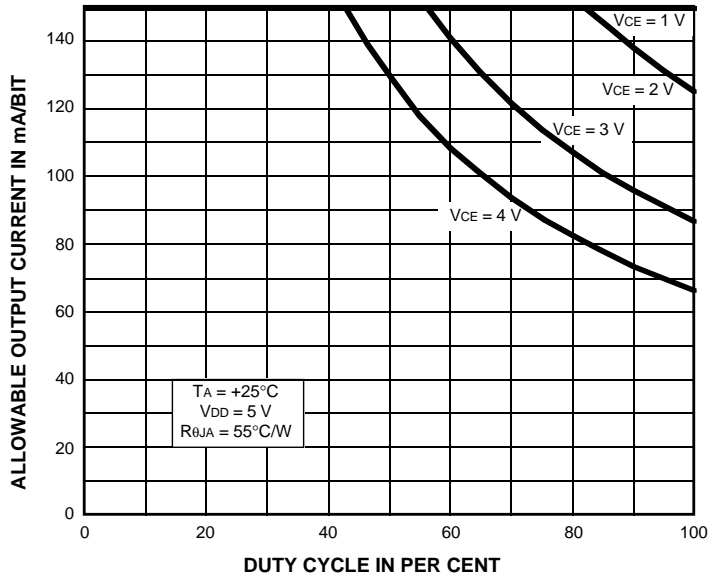
Information present at any register is transferred to the respective latch when the LATCH ENABLE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the LATCH ENABLE is held high. Applications where the latches are bypassed (LATCH ENABLE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, the output source drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

6277 8-BIT SERIAL-INPUT, CONSTANT-CURRENT LATCHED LED DRIVER

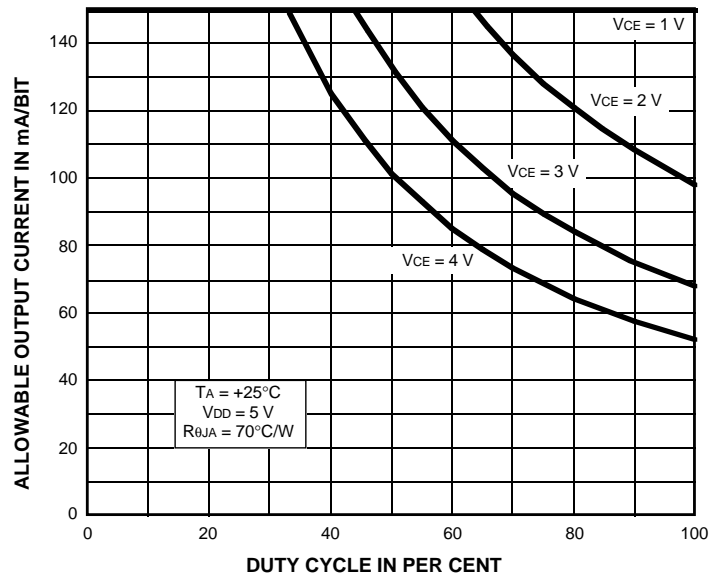
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

A6277xA

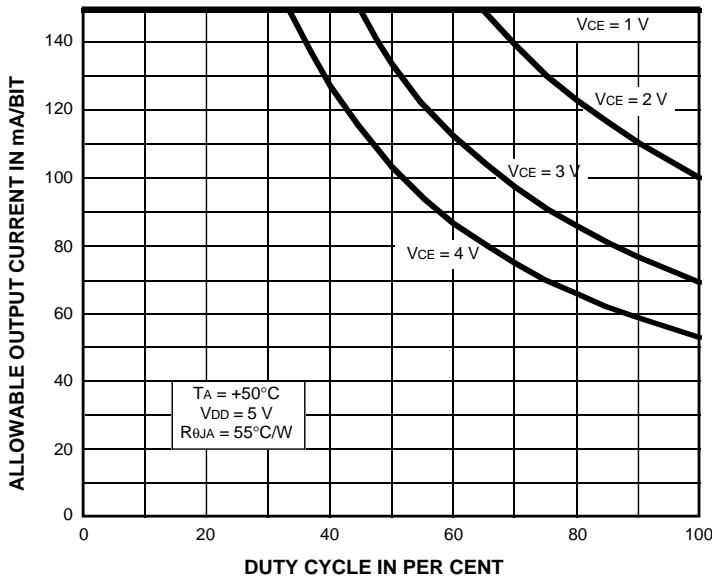


Dwg. GP-062-17

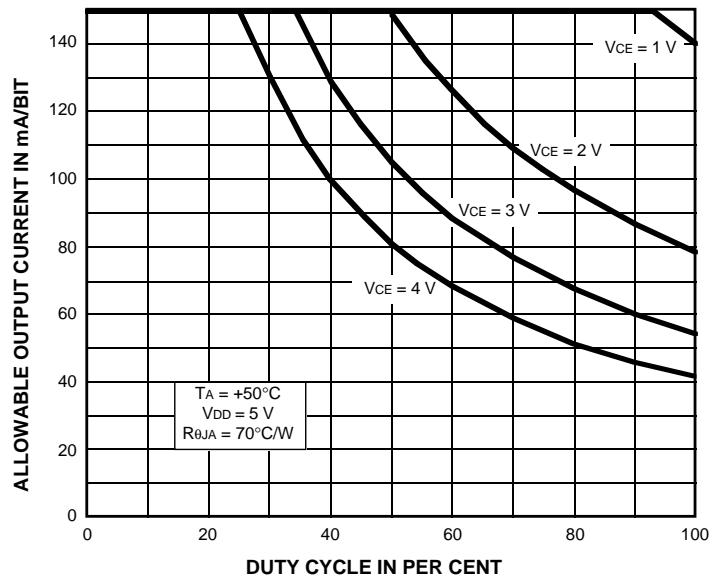
A6277xLW



Dwg. GP-062-16



Dwg. GP-062-15



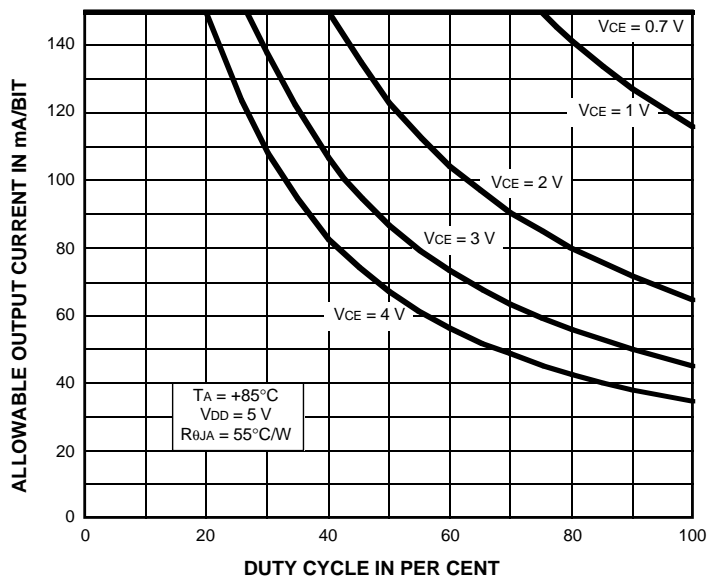
Dwg. GP-062-14

6277

8-BIT SERIAL-INPUT, CONSTANT-CURRENT LATCHED LED DRIVER

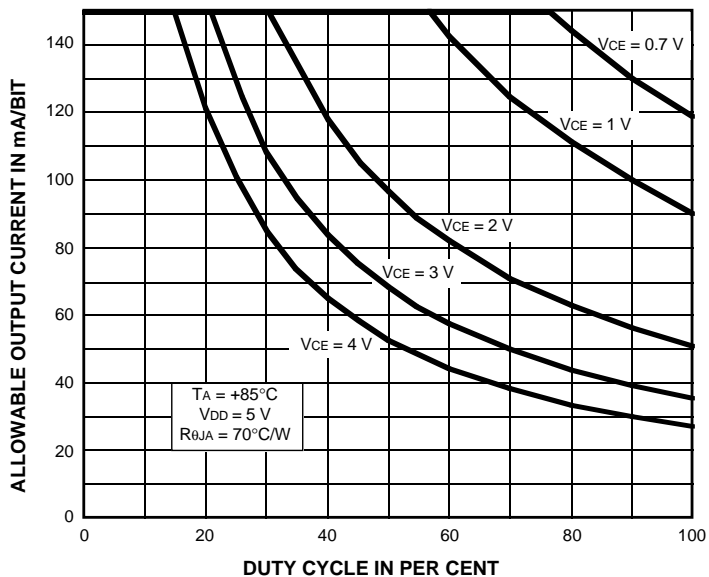
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE (cont.)

A6277xA



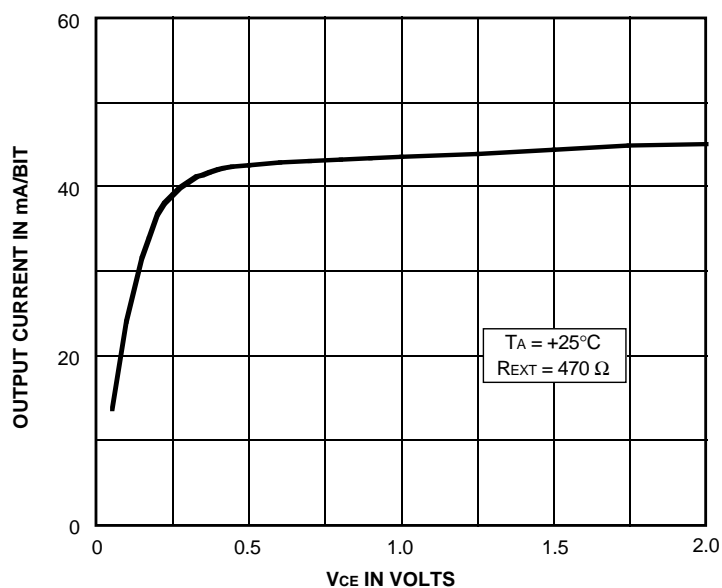
Dwg. GP-062-13

A6277xLW



Dwg. GP-062-12

TYPICAL CHARACTERISTICS



Dwg. GP-063-1

6277
**8-BIT SERIAL-INPUT,
 CONSTANT-CURRENT
 LATCHED LED DRIVER**

TERMINAL DESCRIPTION

Terminal No.	Terminal Name	Function
1	LOGIC GROUND	Reference terminal for control logic.
2	SERIAL DATA IN	Serial-data input to the shift-register.
3	CLOCK	Clock input terminal for data shift on rising edge.
4	LATCH ENABLE	Data strobe input terminal; serial data is latched with high-level input.
5	HIGH/LOW (CURRENT)	Logic low for 100% of programmed current level; logic high for 50% of programmed current level.
6	POWER GROUND	Ground.
7-14	OUT ₀₋₇	The eight current-sinking output terminals.
15	POWER GROUND	Ground.
16	OUTPUT ENABLE	When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
17	SERIAL OUT ₂	CMOS serial-data output (on clock falling edge).
18	SERIAL OUT ₁	CMOS serial-data output (on clock rising edge) to the following shift-registers.
19	R _{EXT}	An external resistor at this terminal establishes the output current for all sink drivers.
20	LOGIC SUPPLY	(V _{DD}) The logic supply voltage. Typically 5 V.

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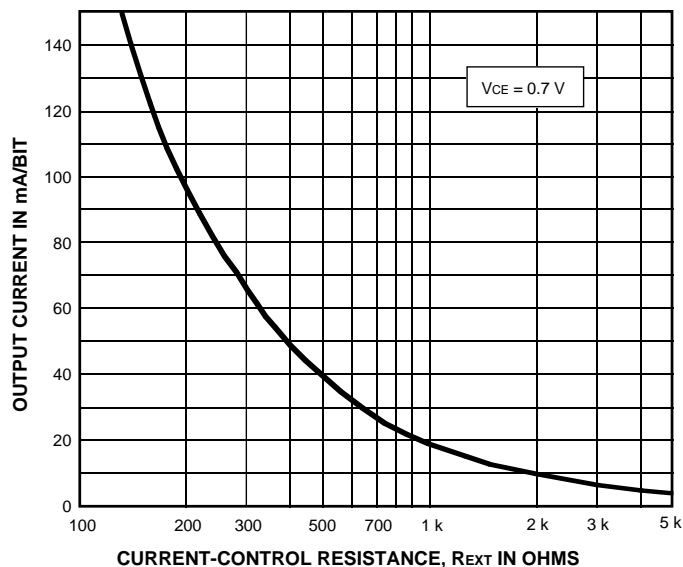
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6277

8-BIT SERIAL-INPUT, CONSTANT-CURRENT LATCHED LED DRIVER

Applications Information

The load current per bit (I_O) is set by the external resistor (R_{EXT}) as shown in the figure below.



Dwg. GP-061-1

Package Power Dissipation (P_D). The maximum allowable package power dissipation is determined as

$$P_D(\max) = (150 - T_A)/R_{\theta JA}$$

The actual package power dissipation is

$$P_D(\text{act}) = dc(V_{CE} \cdot I_O \cdot 8) + (V_{DD} \cdot I_{DD})$$

When the load supply voltage is greater than 3 V to 5 V, considering the package power dissipating limits of these devices, or if $P_D(\text{act}) > P_D(\max)$, an external voltage reducer (V_{DROP}) should be used.

Load Supply Voltage (V_{LED}). These devices are designed to operate with driver voltage drops (V_{CE}) of 0.4 V to 0.7 V with LED forward voltages (V_F) of 1.2 V to 4.0 V. If higher voltages are dropped across the driver, package power dissipation will be increased significantly. To minimize package power dissipation, it is recommended to use the lowest possible load supply voltage or to set any series dropping voltage (V_{DROP}) as

$$V_{DROP} = V_{LED} - V_F - V_{CE}$$

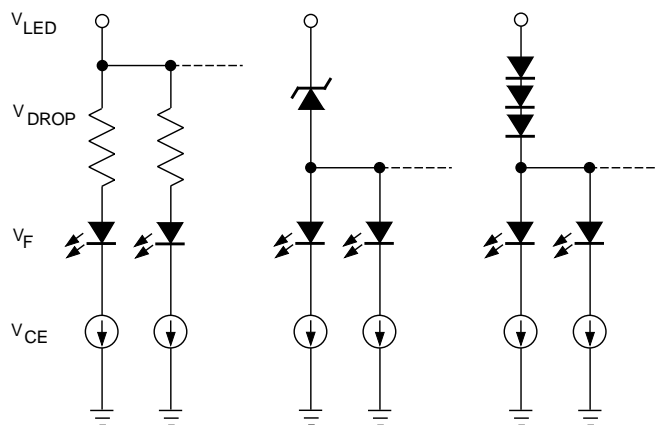
with $V_{DROP} = I_O \cdot R_{DROP}$ for a single driver, or a Zener diode (V_Z), or a series string of diodes (approximately

0.7 V per diode) for a group of drivers. If the available voltage source will cause unacceptable dissipation and series resistors or diode(s) are undesirable, a regulator such as the Sanken Series SAI or Series SI can be used to provide supply voltages as low as 3.3 V.

For reference, typical LED forward voltages are:

Blue	3.0 – 4.0 V
Green	1.8 – 2.2 V
Yellow	2.0 – 2.1 V
Amber	1.9 – 2.65 V
Red	1.6 – 2.25 V
Infrared	1.2 – 1.5 V

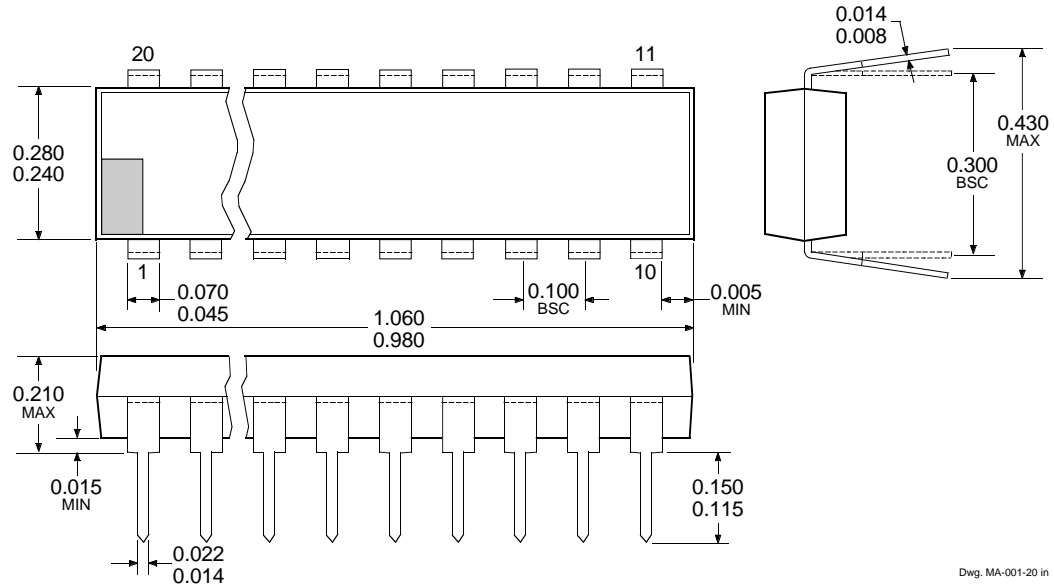
Pattern Layout. This device has separate logic-ground and power-ground terminals. If ground pattern layout contains large common-mode resistance, and the voltage between the system ground and the LATCH ENABLE or CLOCK terminals exceeds 2.5 V (because of switching noise), these devices may not operate correctly.



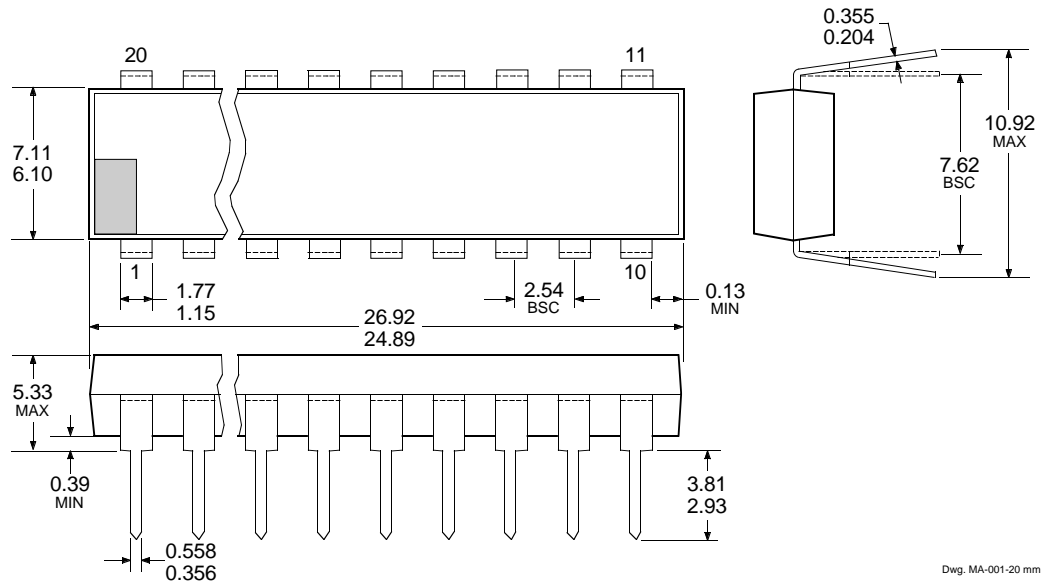
Dwg. EP-064

6277 8-BIT SERIAL-INPUT, CONSTANT-CURRENT LATCHED LED DRIVER

A6277EA Dimensions in Inches (controlling dimensions)



Dimensions in Millimeters (for reference only)



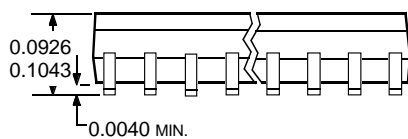
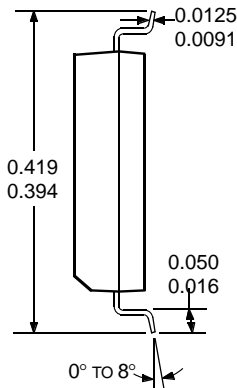
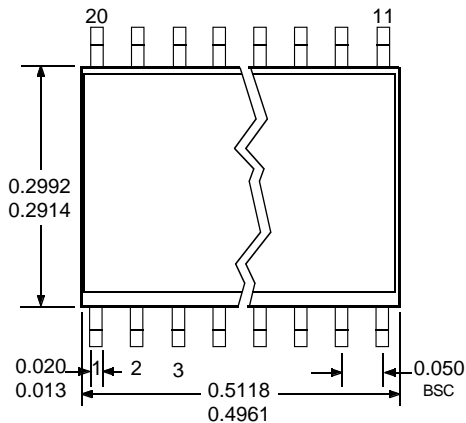
- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 2. Lead spacing tolerance is non-cumulative
 3. Lead thickness is measured at seating plane or below.
 4. Supplied in standard sticks/tubes of 18 devices.

6277

8-BIT SERIAL-INPUT, CONSTANT-CURRENT LATCHED LED DRIVER

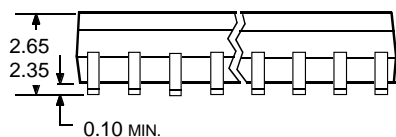
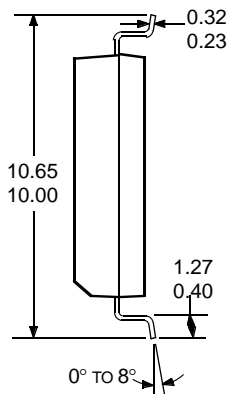
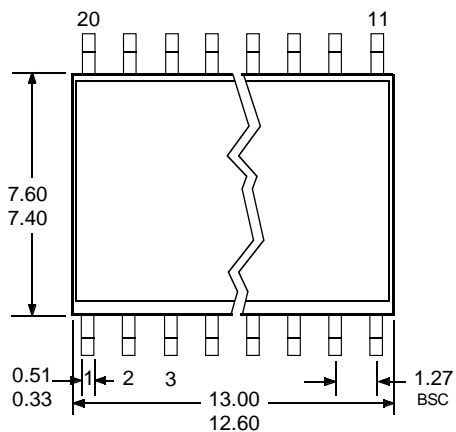
A6277ELW

Dimensions in Inches
(for reference only)



Dwg. MA-008-20 in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-20 mm

- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 37 devices or add "TR" to part number for tape and reel.